REMARKS

Claims 1-5, 7-17 and 19-22 are currently pending in the subject application and are presently under consideration. Claims 1, 14, 17, 19, 21 and 2 have been amended as shown at pages 2-6 of the Reply.

Applicants' representative thanks Examiners Kindred and Lee for the courtesies extended during the telephonic interview conducted on February 11, 2008. Examiners were contacted to discuss the claim rejections under 35 U.S.C. §103(a). Applicants' representative provided further clarification regarding the novelty of the claim limitations. Examiners indicated that further search and consideration was required to determine if the claims would be allowed over the cited prior art.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claims 1-5, 7-17 and 19-22 Under 35 U.S.C. §103(a)

Claims 1-5, 7-17 and 19-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Safranek et al. (US 2004/0193755) in view of Kondratiev et al. (US 6,922,740). It is respectfully submitted that this rejection should be withdrawn for at least the following reasons. Sanfranek *et al.* and Kondratiev *et al.*, alone or in combination, do not teach each and every element of applicants' invention as recited in the subject claims.

> "Under 35 U.S.C. 103 where the examiner has relied on the teachings of several references, the test is whether or not the references viewed individually and collectively would have suggested the claimed invention to the person possessing ordinary skill in the art. It is to be noted, however, that citing references which merely indicated that isolated elements and/or features recited in the claims are known is not a sufficient basis for concluding that the combination of claimed elements would have been obvious. That is to say, there should be something in the prior art or a convincing line of reasoning in the answer suggesting the desirability of combining the references in such a manner as to arrive at the claimed invention... [I]t would not have been obvious to modify [the prior art] ... without using [the patent application's] claims as a guide. It is to be noted that simplicity and hindsight are not proper criteria for resolving the issue of obviousness." *Ex parte Hiyamizu*, 10 USPQ2d 1393 (BPAI 1988).

Independent claim 1 recites *an access data store that stores access information associated with memory, the access data store comprising an access table,* ***the access table comprising a source identifier field, a memory address field and an access attribute field, the access attribute field distinguishes between read, read and write, write, and no access to indicate read, read and write, write, or no access for a combination of source associated with the access attribute and memory address range associated with the access attribute identified in the source identifier field and memory address field****; and a memory controller that employs the access information to determine whether a requested direct memory access is permitted and rejects the requested direct memory access if it is not permitted.*

As conceded in the Office Action, Sanfranek *et al.* does not teach or suggest the aforementioned novel aspects of applicant's invention as recited in the subject claims. The cited art discloses a method for preventing non-CPU devices from accessing protected memory. This is accomplished by maintaining a NODMA memory cache where each bit in the cache represents a page of memory. The setting of the bit (0 or 1) determines if the associated memory page is protected. If a memory access request for a page comes from a non-CPU device and the NODMA cache indicates that the page is protected, the access will be denied. However, this provides very fine control of memory pages, but lacks the combined source, memory, and access type control of the subject claim. Kondratiev *et al.* is cited to make up for the above noted deficiencies of Sanfranek *et al.*, but also fails to teach all novel features of the subject claim. Kondratiev *et al.* teaches a system for controlling DMA access from devices. The Office Action cites Figure 2 and column 4, lines 40-65 as teaching the *source identifier field, memory address field and access attribute field* of the subject claim. However, the cited art discloses a table that contains rows containing device ID field, read memory range field, write memory range field and duration field. This provides an access control list that indicates memory ranges a device is allowed to access. The table *only* indicates memory ranges that are allowed access. It does not provide the ability to directly specify a memory range that is not allowed access. Moreover, read and write access are indicated in two separate fields by specifying a memory address range in each of the two separate read memory range and write memory range fields. This table of the cited reference fails to teach an access attribute field as recited in the subject claim. The access attribute in applicant's claimed invention provides within a single field an indication distinguishing between both allowed and disallowed access information including access type.

This provides allowed and disallowed control information to be stored together, as well as providing both types of information for a single device. For example, the table can have an entry for device A indicating read access for memory range X and another entry for device A indicating no access for memory range Z. In another example, the table could have an entry for device B indicating no access for memory range Y, thereby allowing it access to all memory ranges except Y. Using the combination of a source identifier field, a memory address field and an access attribute field to define allowed and disallowed access provides for more robust and efficient definition of memory access privileges using reduced table space. Sanfranek *et al.* and Kondratiev *et al.* fail to disclose this novel feature discloses in the subject claim.

Furthermore, independent claim 14 recites *a memory controller that includes an access data store comprising an access table,* ***the access table comprising a source identifier field, a memory address field and an access attribute field****, the access attribute field contains an access attribute that distinguishes between read, read and write, write, and no access to indicate read, read and write, write, or no access for a combination of source associated with the access attribute and memory address range associated with the access attribute identified in the source identifier field and memory address field,* ***an access attribute distinguishes from amongst read, read and write, write, and no access to indicate read, read and write, write, or no access for a combination of source and memory address range identified by a source identifier associated with the access attribute and a memory address range associated with the access attribute, wherein the access attribute contains data indicating read when the source identified by the source identifier associated with the access attribute is only permitted to read the memory address range associated with the access attribute, wherein the access attribute contains data indicating write when the source identified by the source identifier associated with the access attribute is only permitted to write to the memory address range associated with the access attribute, wherein the access attribute contains data indicating read and write when the source identified by the source identifier associated with the access attribute is permitted to read and write to the memory address range associated with the access attribute, wherein the access attribute contains data indicating no access when the source identified by the source identifier associated with the access attribute is not permitted access to the memory address range associated with the access attribute****, the memory controller employs the access information to determine whether a requested direct memory access is permitted and rejects the requested*

direct memory access if it is not permitted and allows the requested direct memory access if it is permitted. As discussed above both Sanfranek *et al.* and Kondratiev *et al.* fail to teach or suggest an access attribute that can distinguish between all of read, write, read and write, and no access for a specified source and memory range. The references take a more data intensive approach by either mapping the entire memory space to bit references or requiring separate fields for read and write access. These approaches provide less control for memory access and require more data table space. As recited in the subject claim, the access attribute has specific indicators for each of read, write, read and write, and no access for a specified source and memory range.

Moreover independent 17 recites *receiving a request for a direct memory access transaction, the request comprising a source identifier, at least one memory address, and an* ***access attribute****; and, determining whether the request is permitted based, at least in part on, stored access information and the request, the stored access information comprising at least one source identifier, at least one memory address range and at least one access attribute****, an access attribute distinguishes between read, read and write, write, and no access to indicate read, read and write, write, or no access for a combination of source associated with the access attribute and memory range associated with the access attribute identified by the at least one source identifier and at least one memory address range.*** As noted *supra* both Sanfranek *et al.* and Kondratiev *et al.* fail to teach or suggest an access attribute that can distinguish between all of read, write, read and write, and no access for a specified source and memory range within a single attribute. Sanfranek *et al.* is not concerned with what type of access is allowed, just whether access is allowed or not. Kondratiev *et al.* employs two data fields to indicate read memory range and write memory range. The combination fails to disclose an access attribute that can distinguish between all of read, write, read and write, and no access for a specified source and memory range.

Additionally, independent claim 21 recites *a data field comprising a corrected platform error event, the corrected platform error event being based, at least in part, upon a determination that a requested direct memory access is not permitted, the determination being based, at least in part, upon access information stored in an access table and the requested direct memory access, the access information comprising at least one source identifier, at least one memory address range and at least one access attribute,* ***the at least one access attribute distinguishes from amongst read, read and write, write, and no access to indicate read, read***

and write, write, or no access for a combination of source and memory address range identified by the at least one source identifier and at least one memory address range associated with the at least one access attribute. As previously discussed Sanfranek *et al.* and Kondratiev *et al.*, alone or in combination, fail to teach or suggest an access attribute that can distinguish between all of read, write, read and write, and no access for a specified source and memory range.

Independent claim 22 recites *means for determining whether a requested direct memory access is permitted based, at least in part, upon the stored access information and the request, the stored access information comprising at least one source identifier, at least one memory address range and at least one access attribute,* ***the at least one access attribute distinguishes between read, read and write, write, and no access to indicate one of read, read and write, write, or no access for a combination of source and memory address range identified by the at least one source identifier and at least one memory address range associated with the at least one access attribute.*** Sanfranek *et al.* and Kondratiev *et al.*, alone or in combination, fail to teach or suggest an access attribute that can distinguish between all of read, write, read and write, and no access for a specified source and memory range. As such, the cited references fail to teach all novel aspects of the subject claim.

Accordingly, applicants' representative respectfully submits that Sanfranek *et al.* and Kondratiev *et al.*, alone or in combination, fail to teach or suggest all limitations of applicants' invention as recited in independent claims 1, 14, 17, 21 and 22 (and claims 2-5, 7-13, 15, 16, 19 and 20 that depend there from) and thus fails to make obvious the subject claimed invention. For this reason, this rejection should be withdrawn.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [MSFTP553US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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